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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/087,330	03/01/2002	Kwang-Shik Shin	SAM-0130DIV	4997

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EXAMINER	
TRINH, MICHAEL MANH	
ART UNIT	**PAPER NUMBER**
2822	

DATE MAILED: 12/02/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/087,330	SHIN ET AL.	
	Examiner	Art Unit	
	Michael Trinh	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 September 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

*** This office action is in response to Applicant's amendment filed on September 22, 2003. Claims 1-12 are currently pending.

*** The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 103

1. Claims 1-4,7-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kamiya (6,080,624) taken with Applicant admitted prior art (present specification page 1, line 16 through page 3, line 20; and Figures 1,2A-2B), and Kamiya (5,838,615).

Kamiya et al '624 teach (at Figs 4, 11-14; col 6, line 12 through col 8; Figs 25-30; col 11, line 16 through col 12) a method of fabricating a NAND-type flash memory device comprising at least the step of: forming a plurality of isolation layers 112 running parallel with each other at predetermined regions of a semiconductor substrate; forming a string selection line pattern, a plurality of word line patterns, and a line pattern (Fig 3; col 5, lines 41-67; Fig 25; col 11, lines 16-67) crossing over the plurality of isolation layers 112 and active regions between the plurality of isolation layers; implanting impurities into the active regions among the string selection line pattern, the plurality of word lines pattern and a line pattern, thereby forming drain regions 120b at the active regions adjacent to the string selection line pattern and opposite a line pattern and concurrently forming source regions 120a at the active regions adjacent to a line pattern and opposite the string selection line pattern (Figs 4-12, col 4, line 13 through col 8; and Figs 25-30, col 11, line 16 through col 12) ; forming a first interlayer insulating layer 130 on the entire surface of the substrate including the drain and source regions 120; planarizing and patterning the first interlayer insulating layer 130 to form a slit-type common source line contact holes 130a (col 8, lines 4-6) exposing the source regions 120a and the isolation layers 112 between the source regions 120 (col 8, lines 6-8; Figure 4,11-15); and forming a common source line 121 filling the common source line contact holes 13a, wherein as shown in Figure 12 a top surface level of the common source line 12 is even with a top surface level of the remained first interlayer insulating layer 130, and wherein the contact hole is formed between two layered gated sections. Re claims 2-3 and 8-9, wherein an etch stop layer 119 of silicon nitride having an etch selectivity with respect to the interlayer insulating film 130 is formed on the substrate

including source and drain regions (Fig 5, col 7, lines 10-15 through col 8), and wherein etching and patterning of the interlayer insulating layer 130 exposes the etch stop layer 119 as etch stopper. Re claims 4 and 10, wherein a conductive layer 151 in the slit-type common source line contact hole 130a is planarized until the first interlayer insulating layer 130 is exposed (Fig 12; col 8, lines 1-23).

Kamiya '624 does not mention the common source line adjacent to the ground select line pattern in making the NAND flash memory device, and teach forming the contact hole between two layered gated sections.

However, Applicant admitted prior art teaches (at Figs 1-3; present specification page 1, line 16 to page 3, line 20) a NAND flash memory device including a serial connection of a string selection line pattern 2s for selection transistors (Figs 1,2B), a plurality of word lines pattern (Wp) for cell transistors, and the ground selection line pattern for ground selection transistor, wherein a drain region 7d of the string selection transistor is connected to the bit line 9, and the source region 7s of the ground selection transistor is connected to a common source line 5, and wherein a common source line is formed adjacent to the ground selection line pattern. Kamiya '615 teaches (at Figures 1-5; col 4, line 44 through col 6), right after depositing a first interlayer insulating layer 111, patterning the first interlayer insulating layer 111 to form a split-type common source line contact hole exposing the source regions and the isolation layers 101 between the source regions; and forming a common source line filling the common source line contact hole, wherein a top surface level of the common source line 115 is even with or lower than a top surface level of the remaining first interlayer insulating layer 111 (Figs 2-4; col 5, line 4-57).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the NAND flash memory device of Kamiya '624 by including a ground selection line pattern for ground selection transistor that serially connected with the cell transistors as taught by the Applicant admitted prior art, wherein the common source line is formed adjacent to the ground selection line pattern. This is because of the desirability to complete fabrication the flash memory device so that the data stored in memory cells can be properly operated as a NAND type device. The subject matter as a whole would have been obvious to one of ordinary skill in the art at the time the invention was made to form the NAND

flash memory device of Kamiya '624 by patterning a first interlayer insulating film, right after deposition, to form a split-type common source line contact hole and filling the common source line contact hole, wherein a top surface level of the common source line is even with or lower than a top surface level of the remaining first interlayer insulating layer, as taught by Kamiya '615 (the same inventor of Kamiya '624) This is because of the desirability to form the spit-type common contact hole for the common source line, wherein remaining portions of the first interlayer insulating layer protect the underlying gate sections and alternative method for forming the split-type common contact hole, and wherein processing steps are reduced since planarization of the first interlayer insulating layer is not needed.

2. Claims 1-4,6-10,12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant admitted prior art (present specification page 1, line 16 through page 3, line 20; and Figures 1,2A-2B) taken with Kamiya et al (6,080,624) and Kamiya (5,838,615).

Applicant admitted prior art teaches (at Figs 1A, 2A-2B; present specification page 1, line 16 through page 3, line 21) a method of fabricating a NAND-type flash memory device comprising at least the step of: forming a plurality of isolation layers running parallel with each other at predetermined regions of a semiconductor substrate; forming a string selection line pattern 2s (Figs 1,2B), a plurality of word line patterns (WP) and a ground selection line pattern 2g crossing over the plurality of isolation layers 1a (Fig 2A) and active regions between the plurality of isolation layers 1a; introducing impurities into the active regions among the string selection line pattern 2s, the plurality word lines pattern WP and the ground selection line pattern 2g, thereby forming drain regions 7d at the active regions adjacent to the string selection line pattern 2s and opposite the ground selection line pattern 2g and forming source regions 2s at the active regions adjacent to the ground selection line pattern 2g and opposite the string selection line pattern 2s (Fig 2B); forming a first interlayer insulating layer 4 on the entire surface of the substrate including the drain and source regions; patterning the first interlayer insulating layer 4 to form common source line contact holes exposing the source regions; and forming a common source line 5 filling the common source line contact holes (Fig 2A). Re claim 6, forming a second interlayer insulating layer 6 on the entire surface (Fig 2B, present specification page 2, line 10 through page 3); sequentially patterning the first and second interlayer insulating layers

4,6 to form bit line contact hole exposing the drain regions 7d; forming a bit line contact plug 8a, forming a metal layer 9 thereon, and patterning the metal layer to form a plurality of bit lines crossing over the word lines and the common source line (Figs 1,2B).

Re claims 1 and 7, Applicant admitted prior art teaches forming common source line contact holes, but lacks forming the contact hole as a slit-type common source line contact hole.

However, Kamiya et al '624 teach (at Figs 4, 11-14; col 6, line 12 through col 8; Figs 25-30; col 11, line 16 through col 12) a method for forming a flash memory device by forming a common source line 121 in a slit-type common source line contact hole 130a exposing the source regions 120a and the isolation layers 112 between the source regions 120a (col 8, lines 6-8; Figure 4,11-15), wherein a top surface level of the common source line 12 is even with a top surface level of the remaining first interlayer insulating layer 130 (see Fig 12). Kamiya '615 teaches (at Figures 1-5; col 4, line 44 through col 6), right after depositing a first interlayer insulating layer 111, patterning the first interlayer insulating layer 111 to form a split-type common source line contact hole exposing the source regions and the isolation layers 101 between the source regions; and forming a common source line filling the common source line contact hole, wherein a top surface level of the common source line 115 is even with or lower than a top surface level of the remaining first interlayer insulating layer 111 (Figs 2-4; col 5, line 4-57).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the common contact holes of Applicant admitted prior art by forming the common contact holes as a slit-type common source line contact hole as taught by Kamiya '624 and Kamiya '615, wherein a top surface level of the common source line is even with or lower than a top surface level of the remaining first interlayer insulating layer. This is because it is more reliable by providing an electrical connection to all of source regions through a common large contact hole than through a plurality of small contact holes, wherein by forming a slit-type common contact hole, it prevents the problems of forming no contact holes due to high aspect ratio of the hole depth and thickness of the interlayer insulating layer.

Re claims 2-3,8-9, Applicant admitted prior art lacks forming an etch stop layer having an etch selectivity with respect to and before forming the first interlayer insulating layer 4.

However, Kamiya '624 also teaches (at Fig 5, col 7, lines 10-15 through col 8) forming on the substrate including source and drain regions an etch stop layer 119 of silicon nitride having an etch selectivity with respect to and before forming the first interlayer insulating film 130.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the admitted prior art by forming an etch stop layer before forming the first interlayer insulating layer as also taught by Kamiya '624, because of the desirability to selectively etch the interlayer insulating film and prevent unwanted etching of other layers.

3. Claims 5 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kamiya (6,080,624) and Applicant admitted prior art (present specification page 1, line 16 through page 3, line 20; and Figures 1,2A-2B), or vice versa, and Kamiya '615, as applied to above, and further of Ma et al (5,280,446) or Fazan et al (6,066,528).

The references including Kamiya '624 and Applicant admitted prior art, or vice versa, and Kamiya '615 teach a method as applied above, wherein a common source line of tungsten Kamiya '615 is planarized until the first interlayer insulating film 130 is exposed, and wherein the common source line 5 of Applicant admitted prior art is formed by using a doped polysilicon film (present specification page 3, lines 1-4; Figs 2A-2B).

The references thus lack forming a metal silicide layer on the doped polysilicon film.

However, Ma et al teach (at col 8, lines 29-34) forming a conductive layer for electrical connection to source regions by employing a doped polysilicon with metal silicide on top of it. Fazan et al teach (at Figs 5-12A; col 5, line 40 through col 6) forming a doped polysilicon film in a contact hole formed in a first interlayer insulating film 40; planarizing it to form a doped polysilicon plug 65; and forming a metal silicide 67 on the doped polysilicon plug 65 (Figs 8-10; col 6 lines 1-37).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the common source line of Kamiya '624 or Applicant admitted prior art by employing the doped polysilicon film with a metal silicide on top of it as taught by Ma et al or Fazan. This is because of the desirability to lower resistivity of the polysilicon film and to

reduce RC delay, wherein these conductive layers of low resistivity are alternative and art recognized equivalent for substitution in forming a conductive layer for electrical connection.

Response to Arguments

4. Applicant's remarks filed on September 22, 2003 have been fully considered but they are not persuasive, and also moot in view of the new ground(s) of rejection.

** Applicants' remarks (at remark page 9, last paragraph) that "Kamiya ['624] is directed to a NOR type flash EEPROM..."

In response, it is noted and found unconvincing. Kamiya '624 expressly teaches (at col 11, line 16 through col 12) that "both of the first and second embodiments, described above...can be applied to a NAND type flash EEPROM...".

** Applicants' remarks (at remark page 10) about Kamiya '624 that the top surface of the common source line is "neither even with nor lower than a top surface of the first interlayer insulating layer and is only even with the two layered gate sections 118 because the interlayer insulating film 130 is all eliminated in the contact hole portion".

In response, it is noted and found unconvincing. As clearly shown in Figure 130, portions of the first interlayer insulating layer 130 are remained on the substrate, wherein a top surface of the common source line 121 is even with the top surface of the remained first interlayer insulating layer 130.

Additionally, Kamiya '615, the same inventor of Kamiya '624, teaches (at Figures 1-5; col 4, line 44 through col 6), right after depositing a first interlayer insulating layer 111, patterning the first interlayer insulating layer 111 to form a split-type common source line contact hole exposing the source regions and the isolation layers 101 between the source regions; and forming a common source line filling the common source line contact hole, wherein a top surface level of the common source line 115 is even with or lower than a top surface level of the remaining first interlayer insulating layer 111 (Figs 2-4; col 5, line 4-57).

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Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

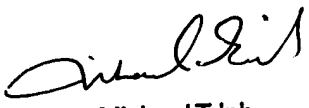
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael M. Trinh whose telephone number is (703) 308-2554. The examiner can normally be reached on M-F from 8:30 Am to 4:30 Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (703) 308-4905. The central fax phone number is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Oacs-6



Michael Trinh
Primary Examiner